Docket No.: SON-2047
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Akihiko Koh et al.

Application No.: 09/802,857 Confirmation No.: 3304

Filed: March 12, 2001 Art Unit: 2192

For: DATA PROCESSING APPARATUS PERFORMING PREDETERMINED DATA PROCESSING IN ACCORDANCE WITH INSTRUCTION CODES READ FROM A PROGRAM MEMORY STORING A PROGRAM

Examiner: M. J. Yigdall

APPELLANT'S BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

This is an Appeal Brief under 37 C.F.R. §41.37 appealing the final decision of the Examiner dated December 16, 2010. Each of the topics required by 37 C.F.R. §41.37 is presented herewith and is labeled appropriately.

A Notice of Appeal is being filed along with this Appellant's Brief.

The Decision of the Board of Patent Appeals and Interferences ("the Board") dated October 31, 2006 *affirmed* the rejections of the Examiner made in the Final Office Action of November 19, 2004.

The Decision on Request for Rehearing of June 27, 2007 ***denied*** a request for rehearing the Decision of October 31, 2006.

A Request for Continued Examination filed on August 21, 2007 requested that the prosecution in the application on appeal be reopened.

The Decision on Appeal of May 14, 2010 ***reversed*** the rejections of the Examiner made in the Final Office Action of December 28, 2007. However, the Decision of May 14, 2010 entered a ***new ground of rejection***.

Subsequent to the Decision of May 14, 2010, an Amendment After Decision on Appeal under 37 C.F.R. 41.50 was filed on June 4, 2010.

This Appellant's Brief is in furtherance of the Final Office Action of December 16, 2010.

Accordingly, the filing of the Appellant's Brief is timely. 37 C.F.R. §1.136.

I. REAL PARTY IN INTEREST

Sony Corporation of Tokyo, Japan ("Sony") is the real party in interest of the present application. An assignment of all rights in the present application to Sony was executed by the inventor and recorded by the U.S. Patent and Trademark Office at **reel 011655, frame 0005.**

II. RELATED APPEALS AND INTERFERENCES

Within the Decision on Appeal dated October 31, 2006, the Board of Patent Appeals and Interferences (the Board) concluded that the Examiner had made a *prima facie* case of obviousness and, thus, sustained the rejection of prior claims 13-25 under 35 U.S.C. §103.

Within the Decision on Rehearing dated on June 21, 2007, the Board has maintained its earlier conclusion rendered in the Decision on Appeal of October 31, 2006 regarding claims 13-25.

Within the Decision on Appeal dated May 14, 2010, the Board concluded that the Examiner had not made a *prima facie* case of obviousness and, thus, ***reversed*** the rejection of prior claims 27, 28, 40, and 45-52 under 35 U.S.C. §103. However, the Decision of May 14, 2010 entered a new ground of rejection.

No other appeals or interferences are believed to directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Within the Final Office Action of December 16, 2010:

> Paragraph 4 of the Office Action indicates a rejection of claim 63 under 35 U.S.C. §112, second paragraph.

Paragraph 6 of the Office Action indicates a rejection of claims 53, 55-59 and 64-69 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,784,537 (Suzuki).

Paragraph 7 of the Office Action indicates a rejection of claims 53-57 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,875,342 (Temple).

Paragraph 9 of the Office Action indicates a rejection of claim 54 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,875,342 (Temple).

Paragraph 10 of the Office Action indicates a rejection of claims 54 and 60-63 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,357,627 (Miyazawa).

Filed along with this Brief is an Amendment After Final Office Action Under 37 C.F.R. 1.116 that includes the cancellation of claims 53-62.

In addition, the Amendment places claims 63 and 64 into independent form.

Although the Amendment includes newly added claims 70-78, these newly added claims are *not intended to be the subject of this appeal*.

Thus, the status of the claims is as follows:

Claims 1-62. (Canceled);

Claims 63-69 (Rejected).

No claims are indicated within the Final Office Action to contain allowable subject matter.

Accordingly, Appellant hereby appeals the final rejection of claims 63-69 which are presented in the Claims Appendix.

IV. STATUS OF AMENDMENTS

Subsequent to the final rejection of December 16, 2010, an Amendment After Final Office Action Under 37 C.F.R. 1.116 has been filed along with this Brief.

No other Amendments have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The following description is provided for illustrative purposes and is not intended to limit the scope of the invention.

Claim 63 is drawn to a data processing apparatus comprising:	
a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a first signal (S_{A1}) and a second signal (S_{A2}) being input to said central processing unit (10) as said interrupt request signal (S_A),	Paragraph beginning at page 24, line 25.
wherein said central processing unit (10) executes a program code, said program code being stored in memory (50) at a program address,	Paragraph beginning at page 15, line 18.
wherein said memory (50) is random access memory (50),	Paragraph beginning at page 25, line 24.
wherein a counter register is located within said random access memory (50), said counter register being incremented when said program address coincides with a first bug address or a second bug address.	

Claim 64 is drawn to a data processing apparatus comprising:	
a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a first signal (S_{A1}) and a second signal (S_{A2}) being input to said central processing unit (10) as said interrupt request signal (S_A),	Paragraph beginning at page 24, line 25.
wherein said central processing unit (10) executes a program code, said program code being stored in memory at a program address,	Paragraph beginning at page 15, line 18.
wherein said first signal (S_{A1}) indicates when said program address and a first bug address coincide, said second signal (S_{A2}) indicating when said program address and a second bug address coincide.	Paragraph beginning at page 24, line 21.

Claim 66 is drawn to a data processing apparatus as set forth in claim 65, wherein a second coincidence detecting circuit (120-2) compares said program address with said second bug address, said second coincidence detecting circuit (120-2) outputting said second signal (S_{A2}) when said program address and said second bug address coincide.	Paragraph beginning at page 24, line 21.

Claim 67 is drawn to a data processing apparatus as set forth in claim 66, wherein a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times.	Paragraph beginning at page 25, line 24.

Claim 69 is drawn to a data processing apparatus as set forth in claim 68, wherein said first buggy part or said second buggy part is selected for correction, said central processing unit (10) using said value to select said first buggy part or said second buggy part.	Paragraph beginning at page 25, line 24.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The issues presented for consideration in this appeal are as follows:

Whether the Examiner erred in maintaining the rejection of claim 63 under 35 U.S.C. §112, second paragraph.

Whether the Examiner erred in maintaining the rejection of claims 53, 55-59 and 64-69 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,784,537 (Suzuki).

Whether the Examiner erred in maintaining the rejection of claims 53-57 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,875,342 (Temple).

Whether the Examiner erred in maintaining the rejection of claim 54 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,875,342 (Temple).

Whether the Examiner erred in maintaining the rejection of claims 54 and 60-63 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,357,627 (Miyazawa).

These issues will be discussed hereinbelow.

VII. ARGUMENT

For at least the following reasons, Appellant submits that the rejection of the claims is both technically and legally unsound and should therefore be reversed.

i. No issues for Appeal remain regarding the rejection of claim 63 under 35 U.S.C. §112, second paragraph.

Page 2 of the Office Action asserts the following:

> *With respect to claim 63 (new), there is insufficient antecedent basis in the claims for "said first bug address" and "said second bug address" such as recited in the claim. The examiner presumes that Applicant intended the claim to recite "a first bug address" and "a second bug address" instead.*

In response, filed along with this Brief is an Amendment After Final Office Action Under 37 C.F.R. 1.116 that includes an amendment to claim 63 by placing that claim into independent form.

The amendment to claim 63 additionally amends claim 63 by replacing "said first bug address" with "a first bug address" and by replacing "said second bug address" with "a second bug address" as suggested by the Examiner.

As a consequence, it is believed that no issues for appeal remain regarding the rejection of claim 63 under 35 U.S.C. §112, second paragraph.

ii. The Examiner erred in maintaining the rejection of claims 53, 55-59 and 64-69 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,784,537 (Suzuki).

A. Standards of review.

The Patent and Trademark Office *may not*, because it may doubt that the invention is patentable, resort to *speculation*, unfounded *assumptions* or *hindsight reconstruction* to supply deficiencies in its factual basis. *In re Warner and Warner*, 154 USPQ 173, 178 (C.C.P.A. 1967).

Instead, determination that a claim is anticipated under 35 U.S.C. §102(b) involves two analytical steps: (1) an interpretation of the claim language; and (2) a comparison of the construed claim to a prior art reference and make factual findings that ***each and every*** limitation is found either expressly or inherently in that ***single prior art reference***. *Yorkey v. Diab*, 94 USPQ2d 1444, 1447 (Fed. Cir. 2010).

Because the hallmark of anticipation is prior invention, the prior art reference—in order to anticipate under 35 U.S.C. §102—must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements "***arranged as in the claim***." *Net MoneyIN Inc. v. VeriSign Inc.*, 88 USPQ2d 1751, 1758 (Fed. Cir. 2008).

The Patent and Trademark Office (PTO) determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "***in light of the specification*** *as it would be* ***interpreted by one of ordinary skill in the art***". *Phillips v. AWH Corp.*, 75 USPQ2d 1321, 1329 (Fed. Cir. 2005).

B. Claims 53 and 55-59 have been cancelled by the Amendment After Final Office Action Under 37 C.F.R. 1.116.

Filed along with this Brief is an Amendment After Final Office Action Under 37 C.F.R. 1.116 that includes the cancellation of claims 53 and 55-59.

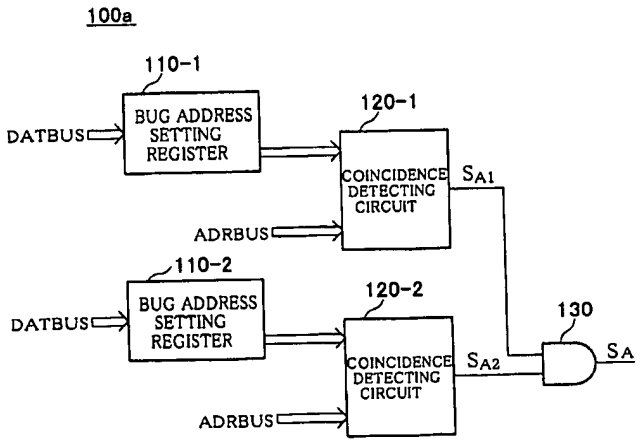
As a consequence, prior claims 53 and 55-59 are *not intended to be the subject of this appeal*.

C. For this rejection only, claims 64 and 65 stand or fall together.

Claim 65 is dependent upon claim 64.

Claim 64 is drawn to a data processing apparatus comprising:	
a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a first signal (S_{A1}) and a second signal (S_{A2}) being input to said central processing unit (10) as said interrupt request signal (S_A),	Paragraph beginning at page 24, line 25.
wherein said central processing unit (10) executes a program code, said program code being stored in memory at a program address,	Paragraph beginning at page 15, line 18.
wherein said first signal (S_{A1}) indicates when said program address and a first bug address coincide, said second signal (S_{A2}) indicating when said program address and a second bug address coincide.	Paragraph beginning at page 24, line 21.

Figure 7 of the specification for the claims on appeal is provided hereinbelow.

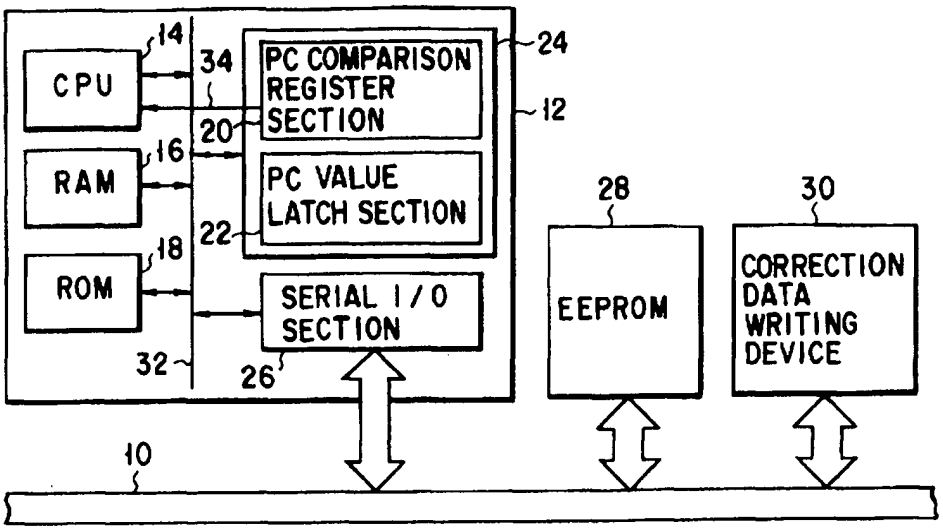


1. U.S. Patent No. 5,784,537 (Suzuki) *fails* to disclose, teach, or suggest first and second signals input to the central processing unit as an interrupt request signal.

Page 4 of the Office Action asserts the following:

> *With respect to claim 64 (new), the rejection of claim 57 is incorporated, and Suzuki further teaches that said first signal indicates when said program address and a first bug address coincide, said second signal indicating when said program address and a second bug address coincide (see, for example, column 6, lines 27-36, which shows that each of the S number of signals indicates that the program address and a correction address coincide).*

In response, Figure 1 of Suzuki is provided hereinbelow.



Suzuki arguably discloses that the PC comparison register section 20 of the ROM correction processing circuit 24 compares a value stored in the PC latch section 22 with an address value (program counter value) of the internal bus 32 (Suzuki at column 4, lines 12-16).

Then, if these values are consistent with each other, the PC comparison register section 20 outputs ***an interruption request signal 34*** to the CPU 14 (Suzuki at column 4, lines 16-18).

Here, Suzuki ***fails*** to disclose, teach, or suggest the interruption request signal 34 being *first and second signals*.

Each and every claimed feature cannot be found within Suzuki.

In accordance with the meaning of ***anticipation*** pursuant to 35 U.S.C. §102, Suzuki ***fails*** to disclose, teach, or suggest *first and second signals input to the central processing unit as an interrupt request signal.*

D. For this rejection only, claim 66 stands or falls alone.

Claim 66 is drawn to a data processing apparatus as set forth in claim 65, wherein a second coincidence detecting circuit (120-2) compares said program address with said second bug address, said second coincidence detecting circuit (120-2) outputting said second signal (S_{A2}) when said program address and said second bug address coincide.	Paragraph beginning at page 24, line 21.

1. Incorporation by reference.

For the purposes of brevity, the arguments presented hereinabove with respect to claim 64 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

2. U.S. Patent No. 5,784,537 (Suzuki) *fails* to disclose, teach, or suggest a *second* coincidence detecting circuit.

Page 5 of the Office Action asserts the following:

> *With respect to claim 66 (new), the rejection of claim 65 is incorporated, and Suzuki further teaches a second coincidence detecting circuit compares said program address with said second bug address, said second coincidence detecting circuit outputting said second signal when said program address and said second bug address coincide (see, for example, ROM correction processing circuit 24 in FIG. 1 and column 4, lines 12-26, which shows that the circuit compares the program address with the correction address and outputs the signal when the program address and the correction address coincide).*

In response, Suzuki arguably discloses that the ***PC comparison register section 20 of the ROM correction processing circuit 24*** compares a value stored in the PC latch section 22 with an address value (program counter value) of the internal bus 32 (Suzuki at column 4, lines 12-16).

However, Figure 1 of Suzuki ***fails*** to depict the ROM correction processing circuit 24 having ***more than one*** PC comparison register section 20.

Instead, only a *single* PC comparison register section 20 is disclosed in Suzuki.

Each and every claimed feature cannot be found within Suzuki.

In accordance with the meaning of ***anticipation*** pursuant to 35 U.S.C. §102, Suzuki ***fails*** to disclose, teach, or suggest *a second coincidence detecting circuit.*

E. For this rejection only, claims 67-68 stand or fall together.

Claim 68 is dependent upon claim 67.

Claim 67 is drawn to a data processing apparatus as set forth in claim 66, wherein a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times.	Paragraph beginning at page 25, line 24.

3. Incorporation by reference.

For the purposes of brevity, the arguments presented hereinabove with respect to claim 66 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

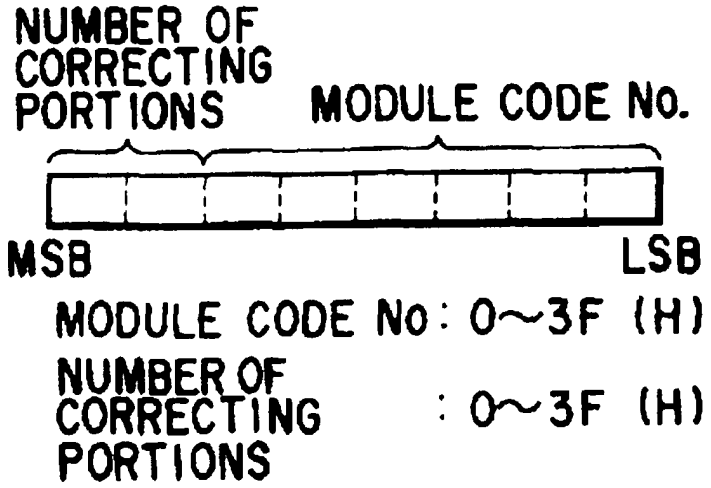
4. U.S. Patent No. 5,784,537 (Suzuki) *fails* to disclose, teach, or suggest a number of times the first or second bug address has coincide with the program address being counted, a value representing the number of times.

Page 5 of the Office Action asserts the following:

With respect to claim 67 (new), the rejection of claim 66 is incorporated, and Suzuki further teaches that a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times (see, for example, FIG. 2B and column 4, lines 41-49, which shows a value in the two most significant bits of a register that represents a number of parts of a program to be corrected, or the number of correction addresses, and see, for example, step S5 in FIG. 4A and step S28 in FIG. 4B, which shows storing the value and counting down

the stored value each time the program address coincides with a correction address, such that the value of the count subtracted from S represents the number of times the addresses coincide).

In response, Figure 2B of Suzuki is provided hereinbelow.



As shown in FIG. 2B, if the lower 6 bits (bit 5 to LSB) are set to a module code No. per one byte and the *residual 2 bits (MSB and bit 6) are set to express the* ***number of correcting portions in the module***, the maximum number of modules to be dealt with becomes 64 (3F (H) to 0 (H)), and the maximum number of correcting portions is four (3 (H) to 0 (H)) (Suzuki at column 4, lines 41-47).

Here, the number of correcting portions in the module depicted within Figure 2B of Suzuki appears to be a pre-set number.

In this regard, the value of the two most-significant bits shown in Figure 2B of Suzuki is set ***prior to*** performing the process depicted within Figures 4A and 4B,

As a consequence, the value of the number of correcting portions within the two most-significant bits shown in Figure 2B of Suzuki ***appears to be a pre-set value that is not*** based upon

any count of the number of times the first or second bug address ***has coincided*** (*not might coincide*) with the program address, especially in the absence of any prior comparison between the bug addresses and a program address.

Moreover, Figure 3 shows an example of a data format reserved in the EEPROM 28 (hereinafter called ROM correction data area) at the time of the interruption processing (Suzuki at column 4, lines 59-61).

First of all, the number of correcting portions and the module code No. are ***stored in a head address "@0xx (H)" of the ROM*** correction data area (Suzuki at column 4, lines 65-67).

Apparently, the values stored within the head address of EEPROM 28 are ***pre-set values*** that are ***not the result*** of the number of times the first and second bug addresses coinciding with the program address.

Suzuki arguably discloses the following in the paragraph beginning at column 5, line 10:

> In the ***example shown in FIG. 3***, it is assumed that three portions to be corrected are present in one module. Due to this, the number of bytes, which is needed to designate the lower address value of the first correction execution interruption address, is 20 bytes. However, the number of use bytes marked by "*" in the figure may not be set since the *number of bytes of each correction program* can be obtained by subtracting the respective correction program head address values from each other. In this example, the ***number of use bytes*** of the first to third correction program areas is a value (38 bytes), which can be obtained by ***subtracting*** *20 bytes from the total number of use bytes (58 bytes)*.

However, Suzuki ***fails*** to teach the "*number of use bytes*" and the "*number of times that the first and second bug addresses coincide with the program address*" as being one in the same.

Instead, the "*number of use bytes*" in Suzuki appears to be the "*number of bytes of each correction program*" (Suzuki at column 5, lines 14-18).

Regarding the flowchart in Figure 4B, Suzuki arguably discloses that then, the stored *number of correcting portions S is decremented* (step S28) (Suzuki at column 6, lines 61-62).

Here, Suzuki ***fails*** to disclose, teach, or suggest the number of correcting portions S representing the number of times that first and second bug addresses coincide with a program address.

Instead, *if the number of correcting portions S* ***is 0***, the processing goes to step S33 since *there is no residual correcting portion* in the subroutine module of code No. m (Suzuki at column 6, lines 65-67).

Furthermore, in step S29, *if the number of correcting portions S is* ***not 0***, the processing goes to step S30 since there is still residual correcting portions (Suzuki at column 6, line 67 to column 7, line 2).

Each and every claimed feature cannot be found within Suzuki.

In accordance with the meaning of ***anticipation*** pursuant to 35 U.S.C. §102, Suzuki ***fails*** to disclose, teach, or suggest *a number of times the first and second bug addresses coincide with the program address being counted, a value representing the number of times.*

F. For this rejection only, claim 69 stands or falls alone.

Claim 69 is drawn to a data processing apparatus as set forth in claim 68, wherein said first buggy part or said second buggy part is selected for correction, said central processing unit (10) using said value to select said first buggy part or said second buggy part.	Paragraph beginning at page 25, line 24.

5. Incorporation by reference.

For the purposes of brevity, the arguments presented hereinabove with respect to claim 66 are incorporated herein by reference.

Additional arguments are provided hereinbelow.

6. U.S. Patent No. 5,784,537 (Suzuki) *fails* to disclose, teach, or suggest the central processing unit using the value to select the first buggy part or the second buggy part.

Page 6 of the Office Action asserts the following:

> *With respect to claim 69 (new), the rejection of claim 68 is incorporated, and Suzuki further teaches or suggests that said first buggy part or said second buggy part is selected for correction, said central processing unit using said value to select said first buggy part or said second buggy part (see, for example, column 6, line 65 to column 7, line 7, which shows that the part of the program to be corrected is selected for correction based on the value).*

In response, Suzuki ***fails*** to disclose, teach, or suggest CPU 14 using the value of the number of correcting portions to select the first buggy part or the second buggy part.

Here, Suzuki sets forth the following in the paragraph beginning at column 6, line 58:

> A jump instruction of "ROM correction data setting processing for next correcting portion" is written to the correction program to be set in the correction program execution area. This instruction is provided to all correction programs. Thereby, ***if the execution of the correction program in step S26 is ended***, the correction

program is jumped to the program of "ROM correction data setting processing for ***next correcting portion***."

Here, Figure 4B of Suzuki ***fails*** to disclose, teach, or suggest CPU 14 using this number of correcting portions S to select the particular correction program.

Each and every claimed feature cannot be found within Suzuki.

In accordance with the meaning of ***anticipation*** pursuant to 35 U.S.C. §102, Suzuki ***fails*** to disclose, teach, or suggest *the central processing unit using the value to select the first buggy part or the second buggy part.*

ii. The Examiner erred in maintaining the rejection of claims 53-57 under 35 U.S.C. §102 as allegedly being anticipated by U.S. Patent No. 5,875,342 (Temple).

A. Claims 53-57 have been cancelled by the Amendment After Final Office Action Under 37 C.F.R. 1.116.

Filed along with this Brief is an Amendment After Final Office Action Under 37 C.F.R. 1.116 that includes the cancellation of claims 53-57.

As a consequence, prior claims 53-57 are *not intended to be the subject of this appeal*.

iii. The Examiner erred in maintaining the rejection of claim 54 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,875,342 (Temple).

A. Claim 54 has been cancelled by the Amendment After Final Office Action Under 37 C.F.R. 1.116.

Filed along with this Brief is an Amendment After Final Office Action Under 37 C.F.R. 1.116 that includes the cancellation of claim 54.

As a consequence, prior claim 54 is *not intended to be the subject of this appeal*.

iv. The Examiner erred in maintaining the rejection of claims 54 and 60-63 under 35 U.S.C. §103 as allegedly being unpatentable over U.S. Patent No. 5,784,537 (Suzuki) in view of U.S. Patent No. 5,357,627 (Miyazawa).

A. Standards of review.

The Patent and Trademark Office has the burden of showing a *prima facie* case of obviousness. *In re Bell*, 26 USPQ2d 1529, 1530 (Fed. Cir. 1993).

Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there *must be some articulated reasoning with some rational underpinning* to support the legal conclusion of obviousness. *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (U.S. 2007).

The Patent and Trademark Office ***may not***, because it may doubt that the invention is patentable, *resort to speculation, unfounded assumptions or hindsight reconstruction* to supply deficiencies in its factual basis. *In re Warner and Warner*, 154 USPQ 173, 178 (C.C.P.A. 1967).

B. Claims 54 and 60-62 have been cancelled by the Amendment After Final Office Action Under 37 C.F.R. 1.116.

Filed along with this Brief is an Amendment After Final Office Action Under 37 C.F.R. 1.116 that includes the cancellation of claims 54 and 60-62.

As a consequence, prior claims 54 and 60-62 are *not intended to be the subject of this appeal*.

G. For this rejection only, claim 63 stands or falls alone.

Claim 63 is drawn to a data processing apparatus comprising:	
a central processing unit (10) configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal (S_A), a first signal (S_{A1}) and a second signal (S_{A2}) being input to said central processing unit (10) as said interrupt request signal (S_A),	Paragraph beginning at page 24, line 25.
wherein said central processing unit (10) executes a program code, said program code being stored in memory (50) at a program address,	Paragraph beginning at page 15, line 18.
wherein said memory (50) is random access memory (50),	Paragraph beginning at page 25, line 24.
wherein a counter register is located within said random access memory (50), said counter register being incremented when said program address coincides with a first bug address or a second bug address.	

1. U.S. Patent No. 5,784,537 (Suzuki) *fails* to disclose, teach, or suggest a counter register being incremented when the program address coincides with a first bug address or a second bug address.

Suzuki is ***silent*** as to *a counter being* ***incremented*** *when the program address coincides with a first bug address or a second bug address.*

2. U.S. Patent No. 5,357,627 (Miyazawa) *fails* to disclose, teach, or suggest a counter being incremented when the program address coincides with a first bug address or a second bug address.

Page 9 of the Office Action asserts the following:

> *However, in an analogous art, Miyazawa teaches a plurality of program correction units, 3C-l to 3C-m, each outputting a signal when a program address and a bug address coincide (see, for example, FIG. 12 and column 9, lines 39-58). The plurality of signals are input to an OR gate 40, and an output from the OR gate 40 is provided as an interrupt request signal (see, for example, FIG. 12 and column 9, line 59 to column 10, line 5, and column 10, lines 32-41). The teachings of Miyazawa provide for correcting a plurality of bugs in the program (see, for example, column 2, lines 9-25).*

In response, Miyazawa arguably discloses the following in the paragraph beginning at column 9, line 41:

> FIG. 12 is a block diagram of the program correction circuit 3C. The program correction circuit 3C has a *plurality of program correction units 3C-l to 3C-m* arranged in correspondence with the number of program data to be corrected. Each of the units 3C-l to 3C-m comprises *a PROM 31 having an address data area 32 and*

> *a vector address area 34, and a comparator 36*. The address data area 32 stores an address of the program memory 2 at which an interruption is to be generated, and the vector address area 34 stores the start address of interruption processing as the vector address. The contents of the program counter 1 are input to all the program correction units 3C-1 to 3C-m, and are compared with data in the address data area 32 by the comparator 36. *When a coincidence is detected* between the two addresses, an output enable signal is supplied to the vector address area 34 in the program correction unit in which the coincidence is detected, and the data output from the vector address area 34 is supplied to a count value change circuit 38.

However, Miyazawa is ***silent*** as to *a counter being* ***incremented*** *when the program address coincides with a first bug address or a second bug address.*

3. Combination of Suzuki and Miyazawa *fails* to disclose, teach, or suggest a counter being incremented when the program address coincides with a first bug address or a second bug address.

Pages 11-12 of the Office Action assert the following:

> *With respect to 63 (new), the rejection of claim 60 is incorporated. To the extent Suzuki in view of Miyazawa* ***does not explicitly describe*** *that a counter register is located within said random access memory, said counter register* ***being incremented*** *when said program address coincides with said first bug address or said second bug address, such an implementation nonetheless would have been obvious to those of ordinary skill in the art.*

Here, the Office Action ***readily admits*** that Suzuki ***fails*** to explicitly disclose a counter being ***incremented*** when the program address coincides with a first bug address or a second bug address.

Likewise, the Office Action ***readily admits*** that Miyazawa ***fails*** to explicitly disclose a counter being ***incremented*** when the program address coincides with a first bug address or a second bug address.

Moreover, Suzuki is ***silent*** as to a counter register being ***incremented***.

Here, Suzuki arguably discloses that on the other hand, if the edge is detected in step S80, the ***position counter is incremented*** (step S88), and a prediction value of a stop position is calculated (step S89) (Suzuki at column 9, lines 52-54).

However, Suzuki ***fails*** to disclose a position counter *being incremented when the program address coincides with a first bug address or a second bug address.*

Nevertheless, pages 12-13 of the Office Action assert the following:

> *In Suzuki, the count (i.e., the counter register) is decremented when the program address coincides with a correction address. However, a person of ordinary skill in the art could, with predictable results, implement the data processing apparatus of Suzuki such that the counter register is incremented rather than decremented. Specifically, with reference to FIGS. 4A and 4B, given the number of correction addresses S, a person of ordinary skill in the art could initialize the value to 0 (rather than S) in step S5, increment (rather than decrement) the stored value in step S28, and check whether the stored value is equal to S (rather than 0) in step S29. Such an implementation is analogous to the one described in Suzuki and provides the intended results. Indeed, as evidenced in the Suzuki reference, incrementing the value of a counter register is within the level of ordinary skill in the art (see, for example, step S88 in FIG. 12B and column 9, lines 52-54). In such an implementation, the stored value (i.e., the value of the counter register) would represent the number of times the addresses coincide.*

In response, Suzuki arguably discloses the following in the paragraph beginning at column 6, line 58:

> In the "ROM correction data setting processing for next correcting portion", data of the register such as the accumulator and data of the partial area of the RAM are saved (step S27) similar to step S1. Then, *the stored number of correcting portions S is* ***decremented*** (step S28). As a result of the decrement, it is checked whether or not the number of correcting portions is 0.

In response, in determining the propriety of the Patent and Trademark Office case for *prima facie* obviousness, it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the proposed substitution or other modification. *In re Taborsky* , 183 USPQ 50, 55 (CCPA 1974).

The mere fact that the prior art could be so *modified* ***would not*** have made the modification obvious unless the prior art suggested the desirability of the modification. *In re Gordon*, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

Here, Suzuki arguably discloses that, then, the stored number of correcting portions S is ***decremented*** (step S28) (Suzuki at column 6, lines 61-62).

However, Suzuki ***fails*** to disclose, teach, or suggest the stored number of correcting portions S being incremented in step S28.

Nevertheless, page 12 of the Office Action asserts that: *However, a person of ordinary skill in the art could, with predictable results, implement the data processing apparatus of Suzuki such that the counter register is incremented rather than decremented.*

At least for the following reasons, it is respectfully submitted that, ***in the absence*** of any disclosure within Suzuki or any other objective evidence, the Office Action merely refers to personal conclusions and hindsight reasoning.

As a rule, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the ***known options*** within his or her technical grasp. *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1397 (U.S. 2007).

Such a combination of familiar elements according to ***known*** methods is likely to be obvious when it does no more than yield predictable results. *KSR at 1389.*

However, the support must have existed at the time the claimed invention was made. *In re Merck & Co., Inc.*, 231 USPQ 375, 379 (Fed. Cir. 1986).

Assertions of technical facts in areas of esoteric technology must always be supported by citation to some reference work recognized as standard in the pertinent art and the appellant given, in the Patent Office, the opportunity to challenge the correctness of the assertion or the notoriety or repute of the cited reference. *In re Pardo and Landau*, 214 USPQ 673, 677 (C.C.P.A. 1982).

Broad conclusory statements, standing alone, are ***not evidence***. *In re Dembiczak*, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999).

Here, **no objective evidence** has been identified within the Office Action *for showing that **incrementing** a counter* when the program address coincides with a first bug address or a second bug address ***would have been know***.

No objective evidence has been identified within the Office Action for showing that *a person of ordinary skill in the art could, with predictable results, implement the data processing apparatus of Suzuki such that the counter register is incremented rather than decremented.*

As explained by Judge Krivak of the Board of Patent Appeals and Interferences in Ex parte Givens, "*a summer is an additive circuit and **not** a subtractive circuit.*" *Ex parte Givens*, Appeal No. 2009-003414, pg. 3, (BPAI, August 6, 2009).

Furthermore, it is ***impermissible*** simply to engage in a ***hindsight reconstruction*** of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps. *In re Gorman*, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991).

To imbue one of ordinary skill in the art with knowledge of the invention, when *no prior art reference or references of record convey or suggest that knowledge*, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 220 USPQ 303, 312-313 (Fed. Cir. 1983).

At least for the following reasons, in the absence of any disclosure within Suzuki, Miyazawa, or any other objective supporting evidence, the line of reasoning within the Office Action appears to have been merely ***an extraction from the Appellant's own specification***.

Appellant's own specification present the following in the paragraph beginning at page 25, line 24:

> Here, in order to execute a plurality of debugged programs in an appropriate order, a branch processing program is provided at the start of the interrupt processing routine for branching to each debugged program. For example, a predetermined memory address is assigned as ***a counter register in the RAM 50***. At the initialization, the counter register is cleared (is set to 0). Each time an interrupt routine is executed, ***the counter register is increased by 1***. The CPU 10 is able to judge the number of times of interrupt, that is, which number bug is being corrected, by the value of the counter register. Therefore, the CPU 10 is able to branch to the correct debugged program accordingly, read the program code, and perform the predetermined processing.

Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. *In re Kahn*, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006).

Either individually or in combination, Suzuki and Miyazawa ***fail*** to disclose, teach, or suggest *a counter being incremented when the program address coincides with a first bug address or a second bug address.*

Conclusion

The claims are considered allowable for the same reasons discussed above, as well as for the additional features they recite.

Reversal of the Examiner's decision is respectfully requested.

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Respectfully submitted,

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CLAIMS APPENDIX

1-62. (Canceled)

63. A data processing apparatus comprising:

a central processing unit configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal, a first signal and a second signal being input to said central processing unit as said interrupt request signal,

wherein said central processing unit executes a program code, said program code being stored in memory at a program address,

wherein said memory is random access memory,

wherein a counter register is located within said random access memory, said counter register being incremented when said program address coincides with a first bug address or a second bug address.

64. A data processing apparatus comprising:

a central processing unit configured to initiate execution of an interrupt processing routine upon a transition of an interrupt request signal, a first signal and a second signal being input to said central processing unit as said interrupt request signal,

wherein said central processing unit executes a program code, said program code being stored in memory at a program address,

wherein said first signal indicates when said program address and a first bug address coincide, said second signal indicating when said program address and a second bug address coincide.

65. A data processing apparatus as set forth in claim 64, wherein a first coincidence detecting circuit compares said program address with said first bug address, said first coincidence detecting circuit outputting said first signal when said program address and said first bug address coincide.

66. A data processing apparatus as set forth in claim 65, wherein a second coincidence detecting circuit compares said program address with said second bug address, said second coincidence detecting circuit outputting said second signal when said program address and said second bug address coincide.

67. A data processing apparatus as set forth in claim 66, wherein a number of times said first and second bug addresses coincide with said program address is counted, a value representing said number of times.

68. A data processing apparatus as set forth in claim 67, wherein said first bug address indicates a starting address for a first buggy part of a program or data, said second bug address indicating a starting address for a second buggy part of said program or data.

69. A data processing apparatus as set forth in claim 68, wherein said first buggy part or said second buggy part is selected for correction, said central processing unit using said value to select said first buggy part or said second buggy part.

EVIDENCE APPENDIX

There is no other evidence which will directly affect or have a bearing on the Board's decision in this appeal.

RELATED PROCEEDINGS APPENDIX

Within the Decision on Appeal dated October 31, 2006, the Board of Patent Appeals and Interferences (the Board) concluded that the Examiner had made a *prima facie* case of obviousness and, thus, sustained the rejection of prior claims 13-25 under 35 U.S.C. §103.

Within the Decision on Rehearing dated on June 21, 2007, the Board has maintained its earlier conclusion rendered in the Decision on Appeal of October 31, 2006 regarding claims 13-25.

Within the Decision on Appeal dated May 14, 2010, the Board concluded that the Examiner had not made a *prima facie* case of obviousness and, thus, ***reversed*** the rejection of prior claims 27, 28, 40, and 45-52 under 35 U.S.C. §103. However, the Decision of May 14, 2010 entered a new ground of rejection.

No other appeals or interferences are believed to directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.